forming a second barrier layer, comprising a second dielectric barrier material different from the first dielectric barrier material, on an upper surface of the first barrier layer overlying the single first dielectric layer, on the side surfaces of the single first dielectric layer defining the first opening and on the bottom of the opening;

etching, with selectivity to the first barrier layer, to remove the second barrier layer from, and stopping on, the upper surface of the first barrier layer, and to remove the second barrier layer from the bottom of the first opening, leaving a portion of the second barrier layer as a liner on the side surfaces of the first dielectric layer defining the first opening; and

filling the opening with metal to form a lower metal feature.

6. (Amended) [The method according to claim 1, further comprising:] A method of manufacturing a semiconductor device, the method comprising:

forming a first dielectric layer overlying a substrate;

forming a first barrier layer, comprising a first dielectric barrier material, on the first dielectric layer;

etching to form a first opening defined by side surfaces of the first dielectric layer and a bottom;

forming a second barrier layer, comprising a second dielectric barrier material different from the first dielectric barrier material, on an upper surface of the first barrier layer overlying the first dielectric layer, on the side surfaces of the first dielectric layer defining the first opening and on the bottom of the opening;

etching, with selectivity to the first barrier layer, to remove the second barrier layer from, and stopping on, the upper surface of the first barrier layer, and to remove the second barrier layer from the bottom of the first opening, leaving a portion of the second barrier layer as a liner on the side surfaces of the first dielectric layer defining the first opening;

filling the opening with metal to form a lower metal feature;

forming a third barrier layer, comprising a third dielectric barrier material different from the first dielectric barrier material, on the first barrier layer and on an upper surface of the lower metal feature;

forming a second dielectric layer on the third barrier layer;

forming a fourth barrier layer, comprising a fourth dielectric barrier material, on the second dielectric layer;

forming a third dielectric layer on the fourth barrier layer;

forming a fifth barrier layer, comprising a fifth dielectric barrier material, on the third dielectric layer;

etching to form a dual damascene opening comprising an upper trench portion defined by side surfaces of the third dielectric layer in communication with a lower via hole defined by side surfaces of the second dielectric layer and a bottom on at least a portion of the upper surface of the lower metal feature;

forming a sixth barrier layer, comprising a sixth dielectric barrier material different from the first, fourth and fifth dielectric materials, on the fifth barrier layer overlying the third dielectric layer, on the side surfaces of the third dielectric layer defining the trench, on the side surfaces of the second dielectric layer defining the via